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ANALYSIS AND PERFORMANCE OF  
PARALLELING CIRCUITS FOR  
MODULAR INVERTER-CONVERTER SYSTEMS

*by Arthur G. Birchenough and Francis Gourash*

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16. Abstract <p>As part of a modular inverter-converter development program, control techniques were developed to provide load sharing among paralleled inverters or converters. An analysis of the requirements of paralleling circuits and a discussion of the circuits developed and their performance are included in this report. The current sharing was within 5.6 percent of rated-load current for the ac modules and 7.4 percent for the dc modules for an initial output voltage unbalance of 5 volts.</p>					
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# ANALYSIS AND PERFORMANCE OF PARALLELING CIRCUITS FOR MODULAR INVERTER-CONVERTER SYSTEMS

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## SUMMARY

Modular high-power solid-state inverter and converter systems were developed on contract using high-frequency pulse-width-modulated inverters and converters. The modular concept permits paralleling of modules for increased system power. Paralleling circuits are required to share the load among the modules. The paralleling circuits developed and an analysis of their requirements, including test results, are presented in this report.

The circuits use feedback techniques and can be used to parallel any number of modules. Only two interconnections are required for converter paralleling and five for the inverters. Experimental data show the load sharing will be within 5.6 percent of rated load for the inverters and 7.4 percent for the converters for an initial output voltage difference of 5 volts. The circuits can be disabled for nonparallel operation and have no noticeable effect on the transient performance.

## INTRODUCTION

The parallel operation of static inverter and converter systems generally requires additional circuitry to force load sharing among the paralleled inverters or converters. This report discusses the requirements, design, and performance of two paralleling circuits developed for use with an ac or dc power system which uses transistorized high-frequency pulse-width-modulated conversion.

A program was initiated to develop high-power three-phase 400-hertz ac and dc power systems. The modular approach to inverter-converter packaging requires the paralleling of standard inverter-converter modules in order to obtain the desired system power output level.

The modular approach provides flexibility in designing to specified power levels because system capacity can be changed by adding or deleting standardized inverter and converter modules. It can also reduce development time and costs, since developed and tested off-the-shelf modules can be used, and it should facilitate maintenance through the use of standard replacement modules, particularly in manned missions where such maintenance is feasible.

The paralleled module approach, however, requires the use of control, protection, and load-division circuits. The overall program included development of breadboards of the basic inverter and converter circuits, automatic paralleling, control and protection circuits, and a visual annunciator to monitor system operation. The basic design and construction was performed by the Westinghouse Research and Development Laboratories, Pittsburgh, Pennsylvania, and the Westinghouse Aerospace Electrical Division, Lima, Ohio, under Contract NAS3-9429. Design modifications and testing were then performed at the Lewis Research Center. This report is concerned only with the paralleling circuits, and a description of the operation of the circuits is presented. The breadboard circuits were tested, and the results were compared to the analytical predictions.

The basic inverter-converter circuits and the modular concept have been reported (refs. 1 and 2). Each basic inverter or converter module was rated for 833 watts, single-phase ac at 120 volts, 400 hertz, or 150 volts dc. The ac modules could be connected for three-phase operation. The design goal was to develop paralleling circuits using feedback techniques to obtain current balance within 10 percent of the rated full-load current of each module.

## PARALLELING CONSIDERATION FOR INVERTER-CONVERTER SYSTEMS

Design of a paralleling circuit requires an analysis of the parameters which affect load sharing. A general dc-dc or dc-ac converter system is represented in figure 1. It consists of an ideal converter, its internal impedance  $Z_{int}$ , and a feedback system. The ideal converter is a gain block  $K_1$ , which amplifies the feedback voltage  $V_F$ . Block  $K_2$  is an attenuator for the output voltage, which is compared to the reference or set point  $V_{sp}$ . The paralleling signal  $V_p$  is also added in at this point. The ideal converter output voltage is also affected by the supply voltage  $E_{dc}$ . This effect is represented by  $(\partial E_{int})/(\partial E_{dc})E_{dc}$ , where  $E_{int}$  is the Thevenin equivalent voltage, and  $Z_{int}$  is the Thevenin equivalent impedance. The converter output current is  $I_o$ , and  $\bar{I}_o$  is the average of all the paralleled converter output currents. The Thevenin equiv-

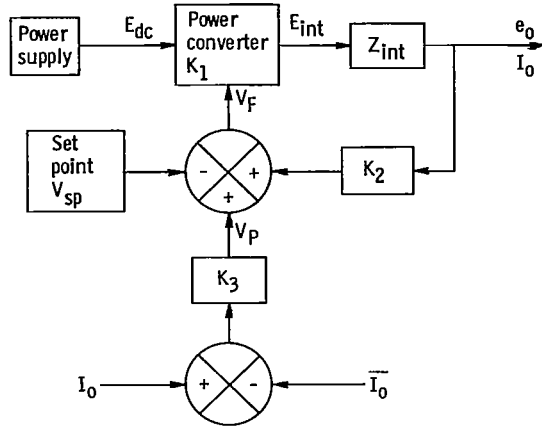


Figure 1. - Block representation of a converter.

alent voltage  $E_{int}$  can be expressed in terms of the quantities shown in figure 1:

$$E_{int} = K_1 \left[ e_o K_2 + (I_o - \bar{I}_o) K_3 - V_{sp} \right] + \frac{\partial E_{int}}{\partial E_{dc}} E_{dc} \quad (1)$$

and

$$e_o = E_{int} - I_o Z_{int} \quad (2)$$

These equations can be used to analyze the effects of any or all of the parameters on the current sharing. If all these parameters are equal for all the paralleled converters, then there would be no unbalance and a paralleling circuit would not be required. The following analysis is concerned only with the effect of the output voltage set point  $V_{sp}$ , since it is the major cause of unbalance for this inverter-converter system.

If equations (1) and (2) are written with the subscript  $A$  to denote a parameter of the  $A^{th}$  converter and the gains and impedances are considered equal (i. e.,  $K_{1,A} = K_1$ ,  $K_{2,A} = K_2$  and  $Z_{int,A} = Z_{int}$ , etc.), then

$$E_{int,A} = K_1 \left[ e_{o,A} K_2 + (I_{o,A} - \bar{I}_o) K_3 - V_{sp} \right] + \frac{\partial E_{int}}{\partial E_{dc}} E_{dc,A} \quad (3)$$

and

$$e_{o,A} = E_{int,A} - I_{o,A} Z_{int} \quad (4)$$

Let

$$\bar{X} = \frac{X_A + X_B + X_C + \dots + X_n}{n}$$

then  $\bar{X}$  is the average, and from equation (3)

$$\begin{aligned} \overline{E_{int}} &= \frac{1}{n} \sum_{j=A}^n E_{int,j} \\ &= K_1 [\bar{e}_o K_2 - \bar{V}_{sp}] + \frac{\partial E_{int}}{\partial E_{dc}} \bar{E}_{dc} \end{aligned} \quad (5)$$

and from equation (4)

$$\bar{e}_o = \bar{E}_{int} - \bar{I}_o Z_{int} \quad (6)$$

Subtracting equation (5) from equation (3) and equation (6) from equation (4) gives

$$\begin{aligned} E_{int,A} - \bar{E}_{int} &= K_1 [(e_{o,A} - \bar{e}_o) K_2 + (I_{o,A} - \bar{I}_o) K_3 - (V_{sp,A} - \bar{V}_{sp})] \\ &\quad + \frac{\partial E_{int}}{\partial E_{dc}} (E_{dc,A} - \bar{E}_{dc}) \end{aligned} \quad (7)$$

and

$$e_{o,A} - \bar{e}_o = E_{int,A} - \bar{E}_{int} - (I_{o,A} - \bar{I}_o) Z_{int} \quad (8)$$

When the converters are paralleled, the input and output busses are connected together,

so  $e_{o,A} = e_{o,B} = \bar{e}_o$  and  $E_{dc,A} = E_{dc,B} = \bar{E}_{dc}$ . Therefore, equations (7) and (8) reduce to

$$E_{int,A} - \bar{E}_{int} = K_1 [(I_{o,A} - \bar{I}_o)K_3 - (V_{sp,A} - \bar{V}_{sp})] \quad (9)$$

and

$$E_{int,A} - \bar{E}_{int} = (I_{o,A} - \bar{I}_o)Z_{int} \quad (10)$$

If we define  $\Delta X_A = X_A - \bar{X}$  and combine equations (9) and (10),

$$\Delta I_{o,A} = \frac{K_1 \Delta V_{sp,A}}{K_1 K_3 - Z_{int}} \quad (11)$$

where  $\Delta I_{o,A}$  is the unbalance current. The unbalance current is zero only if  $\Delta V_{sp}$  is zero, and the unbalance is proportional to  $\Delta V_{sp}$ . Typically  $K_1 K_3$  much larger than  $Z_{int}$ , so

$$\Delta I_{o,A} \approx \frac{\Delta V_{sp}}{K_3} \quad (12)$$

An approximately parallel discussion is given in references 3 and 4.

## DC TO DC CONVERTER PARALLELING

The converter paralleling circuit developed is shown in figure 2. It consists of a current transducer which produces a voltage proportional to the converter output current. This voltage is then compared to the average of all the paralleled converter current transducer outputs, and the difference is amplified.

The current transducer uses a push-pull magnetic amplifier (mag-amp) consisting of saturable transformers  $T_1$  and  $T_2$ . Transformer  $T_3$  supplies the excitation, a 10-kilohertz square wave. The variable resistor  $R_1$  is used to adjust the mag-amp bias current to linearize the transducer output. The voltage across  $R_2$  is proportional to the converter output current. Point Y, one end of  $R_2$ , is connected to the point Y on each of the other paralleling circuits. The voltage at point Y, referenced to ground, is propor-

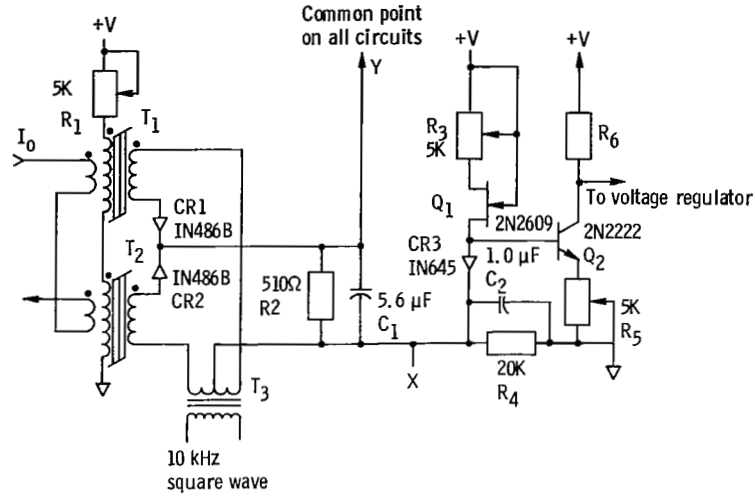


Figure 2. - Load unbalance sensing circuit for dc to dc converter.

tional to the average output current of the paralleled converters. If a particular converter's output is not equal to the output of the other converters, it will have an error voltage from point X to ground. This error is amplified by  $Q_2$  and combined with the output voltage feedback signal. In the initial setup  $R_3$  is adjusted for equal voltages at point X, before the Y's are tied together, and  $R_5$  is adjusted for the correct converter output voltage before paralleling. The forward biased diode CR3 provides temperature compensation for the base emitter voltage of  $Q_2$ .

Independent operation can be restored by disabling the current transducers; this requires changing the bias or removing the excitation. Only two interconnections, a ground and point Y, are required between modules.

There are two major sources of error introduced by this circuit. The first error is due to the current transducers not being matched. This mismatch causes an error in the sensing of the output current, which in turn causes the paralleling circuit to attempt to regulate to an unbalance current. The second error is drift in the amplifier, primarily the  $Q_1 - R_3$  current source, which causes an effect in the output ( $V_p$ ) of the paralleling circuit. Therefore,

$$V_p = K_{3,A} \Delta I_{O,A} + V_{\text{offset}} \quad (13)$$

and

$$V_F = K_3 e_o + (I_{O,A} - \bar{I}_O) K_3 + V_{\text{offset}} - V_{sp} \quad (14)$$



Thus, this offset voltage, caused by the circuit drift, appears the same as a change in  $V_{sp}$  and causes a change in the output voltage, even when it is not in parallel operation, and also causes a current unbalance. Current transducer unbalance causes a term in  $V_p$  similar to

$$V_p = K_3(K_4 I_{O,A} - \bar{I}_O) \quad (15)$$

which does not affect the output voltage.

Variations in the converter parameters, such as internal impedance  $Z_{int}$ , supply sensitivity  $\partial E_{int}/\partial V_{dc}$ , the no-load open-loop voltage regulator gain  $\partial E_{int}/\partial V_O$  etc., and the paralleling circuit gain  $\partial E_{int}/\partial \Delta I$  have little effect since they are inside the feedback loop (fig. 1). These effects can be reduced by increasing the paralleling circuit gain.

## DC TO AC INVERTER PARALLELING

The block diagram of figure 1 and the equations developed from it apply for inverters, except for some phase effects which must be considered. One phase problem is the phase shift between the internal voltage  $E_{int}$  of the inverters. If the internal voltages are not precisely in phase (synchronized), then there will be a voltage difference  $\Delta E_{int}$  as illustrated in figure 3. This  $\Delta E_{int}$  cannot be eliminated by changing the

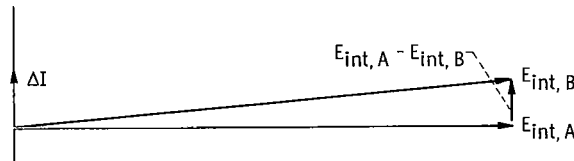


Figure 3. - Differential internal voltage caused by inverter internal phase shift.

magnitudes of the output voltage so an unbalance current results. The phase must be controlled, either by a feedback technique or by a synchronizing signal. In these inverters, the frequency reference signals are synchronized for all the paralleled inverters, and the phase shift in the inverter, largely due to the output filter, is held to a small value, typically  $\pm 1/2^\circ$ .

If it is assumed that the internal voltages are in phase and the internal impedance is resistive, then the unbalance current will be in phase with the internal voltage. The output current of each inverter is

$$\bar{I}_{O,A} = \frac{E_{\text{int},A} - \bar{e}_o}{Z_{\text{int}}} \quad (16)$$

and

$$\bar{I}_O = \frac{\overline{E_{\text{int}}} - \bar{e}_o}{Z_{\text{int}}} \quad (17)$$

Therefore,

$$\Delta I_A = \frac{E_{\text{int},A} - \overline{E_{\text{int}}}}{Z_{\text{int}}} \quad (18)$$

All these quantities are vectors, but since  $E_{\text{int}}$  is in phase with  $\overline{E_{\text{int}}}$  and  $Z_{\text{int}}$  is not reactive, the  $\Delta I$  is in phase with  $E_{\text{int},A}$ . If  $Z_{\text{int}}$  is small compared to the load impedance, then  $E_{\text{int}}$  is nearly in phase with  $e_o$  and  $\Delta I$ , regardless of the load power factor, and this second possible phase problem can be ignored. If  $Z_{\text{int}}$  is not resistive, there will be a phase shift between  $\Delta I$  and  $e_o$ . An R-C lead or lag network could be used to cancel this phase shift, but phase shifts of  $\pm 25^\circ$  can generally be ignored. This magnitude of phase shift results only in an effective decrease (of less than 10 percent) in the paralleling circuit gain. The internal impedance of the test inverters was resistive.

The inverter paralleling system (shown in fig. 4) consists basically of a ring of current transformers whose secondaries are connected in series. These transformers are identical so a current  $I_O(N_p/N_s)$  flows in each secondary, where  $N_p/N_s$  is the turns ratio and  $I_O$  is the output current of the inverter.

The feedback voltage  $V_p$  can be found by first determining the current  $I_R$  which flows in the burden. This analysis assumes no current flows into  $T_2$ . The loading effect of  $T_2$  appears only as a slight reduction in the value of the burden resistor. It can be seen from figure 4 that

$$\frac{N_p}{N_s} I_{O,A} = I_s + I_{R,A} \quad (19)$$

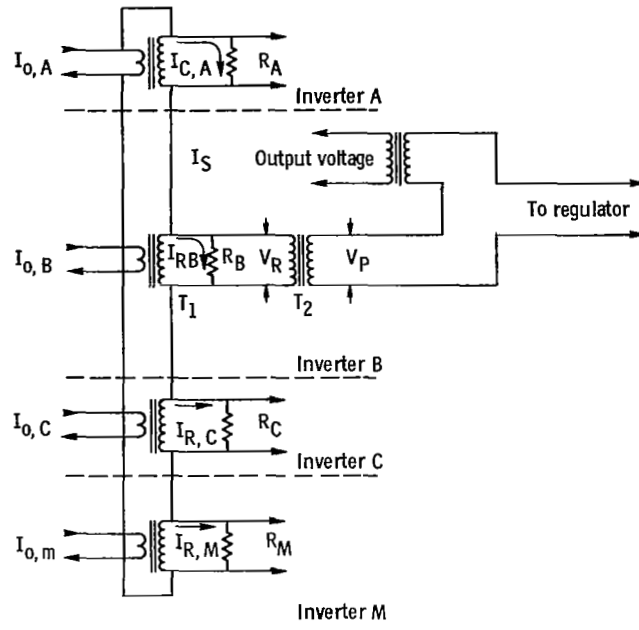


Figure 4. - Inverter paralleling system.

where  $I_s$  is a current which circulates around the ring:

$$\begin{aligned} \frac{1}{N} \sum_{j=A}^n \frac{N_p}{N_s} I_{Oj} &= \frac{N_p}{N_s} \bar{I}_O \\ &= I_s + \frac{1}{n} \sum_{j=A}^n I_{Rj} \end{aligned} \quad (20)$$

From Kirchoff's voltage law,

$$\sum_{j=A}^n V_{Rj} = 0 \quad (21)$$

where  $V_R$  is the voltage across each burden. Since

$$V_R = RI_R \quad (22)$$

then

$$\begin{aligned}\sum_{j=A}^n I_{R_j} &= \frac{1}{R} \sum_{j=A}^n V_{R_j} \\ &= 0\end{aligned}\tag{23}$$

so from

$$I_s = \frac{N_p}{N_s} \bar{I}_o\tag{24}$$

then

$$\begin{aligned}I_{R,A} &= \frac{N_p}{N_s} (I_{o,A} - \bar{I}_o) \\ &= \frac{N_p}{N_s} (\Delta I_{o,A})\end{aligned}\tag{25}$$

Assuming a turns ratio  $N'_s/N'_p$  for  $T_2$  gives

$$V_p = \frac{N'_s}{N'_p} V_R\tag{26}$$

and

$$V_{p,A} = \frac{N_p}{N_s} \frac{N'_s}{N'_p} R \Delta I_{o,A}\tag{27}$$

This voltage is added to the output voltage by transformer  $T_2$ .

Unequal turns ratios in the current transformer will cause the circuit to regulate to a slightly unbalanced output current. Components  $R_1$ ,  $T_1$ , and  $T_2$  affect only the gain, and there are no drift problems as in the converter paralleling problems which affect the output voltage. The circuit can be disabled by shorting the current transformer secondary in each inverter, or by saturating the current transformer core by applying a bias to an auxiliary winding. Both methods were successfully used in this program.

The inverter paralleling circuit required four interconnections between inverters and a ground. The four interconnections are used for the frequency reference signal, a synchronizing signal, and the two current transformer connections.

## APPARATUS AND PROCEDURE

The test circuit for all the paralleling tests is shown in figure 5. Both units were operated from a common input power source, and the synchronizing buses from each

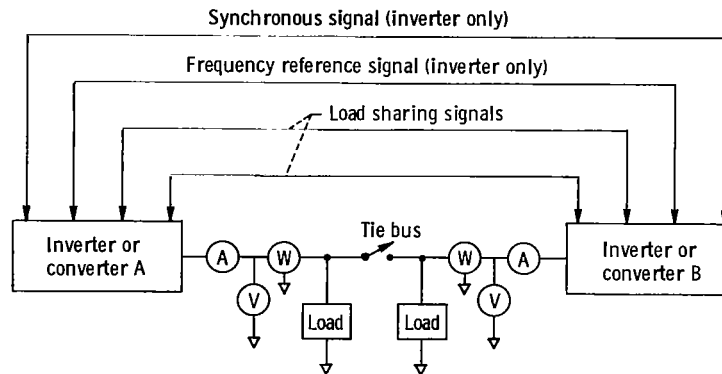


Figure 5. - Block diagram of test setup for paralleling ac or dc system.

inverter were connected together. Each inverter has a frequency reference, but for synchronized operation the reference from one inverter is used to control all the inverters. The converter system does not require synchronization. Output voltage, current, and watts were measured for each converter or inverter. Also, the tie bus could be opened to test the open-loop gain of the current sharing regulators.

The converter and inverter modules including their paralleling circuits were forced-air-cooled breadboards operating at room ambient temperature.

The feedback circuits gains were adjusted for matched regulation curves before paralleling. The output voltage set points were varied to obtain the initial output voltage offset. The modulation controls in the inverter could be adjusted to change the relative phase shift. Load sharing performance is reported for only pairs of inverters or converters. Several units were then paralleled to verify stability and multiple unit parallel operation.

## RESULTS AND DISCUSSION

### Paralleled Converter Performance

The performance of two converters operating in parallel is shown in figure 6. The lower curve shows the performance if the output voltages are precisely balanced at no load with the tie bus open and then paralleled. This condition, balanced output voltages, results in  $\Delta V_{sp,A} = 0$  in equation (11), which is restated as

$$\Delta I_{O,A} = \frac{K_1 \Delta V_{sp,A}}{K_1 K_3 - Z_{int}} \quad (11)$$

If  $\Delta V_{sp,A} = 0$ , then from equation (11)  $\Delta I_{O,A}$  must also be zero. The unbalance indicated in the lower curve of figure 6 is not predicted by equation (27) but is due to cur-

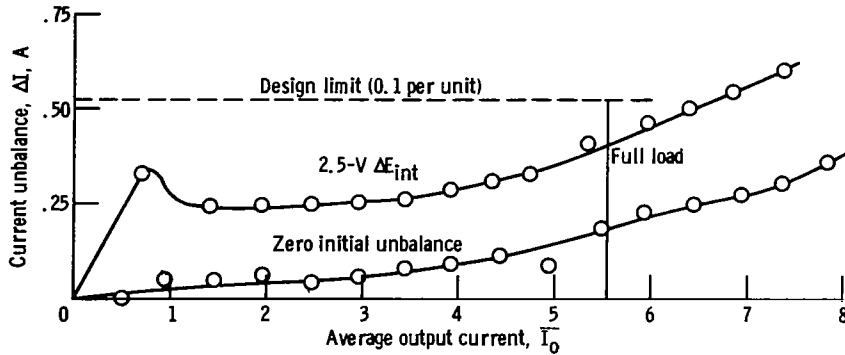


Figure 6. - Current unbalance for two parallel converters.

rent transducer unbalance and the slight difference in converter parameters. At the full rated converter output current of 5.5 amperes, the unbalance is 0.21 ampere or 3.8 percent of full load. The design goal for maximum unbalance is 10 percent per unit (full load) current.

The upper curve in figure 6 shows the additional effect of an initial 2.5 volt  $\Delta E_{int}$ . Equation (11), using previously determined (ref. 1) converter parameters, predicts a paralleling circuit gain  $K_3$  of -10.4 volts per ampere to limit the unbalance to 0.1 per unit current. The experimentally determined gain for one converter (shown in fig. 7) varies between -9.3 and -15 volts per ampere. The gain was determined by operating the converters with the paralleling circuits operating but the output busses unparalleled. Unbalance was controlled by varying the loads independently, and the output voltage dif-

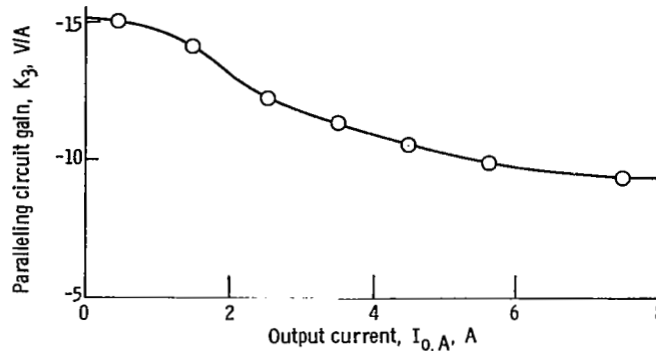


Figure 7. - Converter paralleling circuit gain as function of load.

ference was then measured. A correction due to the effect of  $Z_{int}$  was also required.

The variation in gain is not important, as long as the gain is approximately the desired 10.4 volts per ampere. However, variation in the gain-output current characteristic between different converters accounts for the error shown in the lower curve of figure 6. The additional error due to initial unbalance agrees closely with the prediction of equation (14). An initial output voltage unbalance of 5 volts,  $\Delta E_{int} = 2.5$  volts, results in a total unbalance of 0.4 ampere or 7.2 percent of the full-load current.

The internal impedance ( $Z_{int}$ ) of the converter is approximately 2 ohms from full load to 20-percent load and then increases rapidly to 500 ohms at 3.0-percent load. This increase in  $Z_{int}$  accounts for the decreased unbalance current below a 0.5-ampere load current. The difference in the point at which each converter's output impedance begins increasing may cause the increased unbalance around an 0.8-ampere average output current.

A major problem in the paralleling circuit was drift, primarily in the  $R_3 - Q_1$  current source. This drift caused day to day variations in the output voltage, in a paralleled or nonparalleled mode, of 5 volts.

Because of the large time constant ( $>100$  msec) of the output filter, the load switching had no noticeable effect on the transient performance. Switching in and out of parallel operation was stable for all loads from open circuit to short circuit.

Large capacitor loads as well as the output filter capacitors of other converters in a paralleled system would cause output transistor failures in the converter due to the slow response of the over current circuit. This was not a fault of the paralleling circuit.

The six available converters were operated in parallel. Load sharing was within the specified 10 percent, but the output filter capacitance had to be reduced to eliminate failures as noted previously.

## Paralleled Inverter Performance

The ac paralleling circuit is less complex and more accurate (typically 5.6 as against 7.4 percent current unbalance for the dc circuit) than the dc circuit. Also, it requires no external power supply, and it consumes a maximum of 1/4 watt from the inverter output. The performance of the system with matched no-load output voltage and no phase shift in the internal voltage ( $E_{int}$ ) is shown in figure 8. The maximum unbalance ( $\Delta I$ ) is approximately 0.12 ampere or 1.2 percent of the full-load current (9.8 A at 0.7 power factor). This slight error is probably the result of current trans-

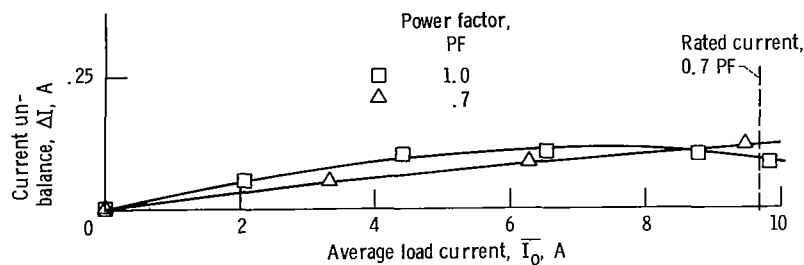


Figure 8. - Current unbalance for two parallel inverters.

former and inverter parameter ( $Z_{int}$ ,  $K_1$ ,  $K_3$ ) differences. Figure 9 shows the effects of both an initial voltage and a phase unbalance. A phase shift results in a circulating current that flows between the two inverters at  $90^\circ$  to the output voltage (fig. 3), which the paralleling circuit cannot correct. The effect of this circulating current on the total output current of the inverter decreases as the load increases because there is a large phase difference between the load current and the circulating current, which are added vectorially. The unbalance in figure 9 does not decrease as the load increases as would be predicted, probably because of other unbalances (fig. 8).

An initial output voltage unbalance caused an error of approximately 0.35 ampere (3.5 percent of rated full-load current) as shown in figure 9. The paralleling circuit has a gain of approximately 6 volts per ampere ( $\partial E_{int} / \partial \Delta I_O$ ). When this gain and the known inverter parameter are used, the current unbalance for a 2.5-volt  $\Delta E_{int}$  should be 0.42 ampere (4.2 percent of full-load current) independent of the load. The two inverters were tested with the load varying between 0 and 150 percent rated, the power factor varying from 0.05 to 1.0 for a 5-volt initial unbalance ( $2.5 \text{ V } \Delta E_{int}$ ), and a phase shift of  $1^\circ$ . The maximum unbalance was 0.55 ampere or 5.6 percent.

Transient response of a parallel inverter system was similar to a nonparallel system. Load switching transients were not shared because the paralleling circuit was



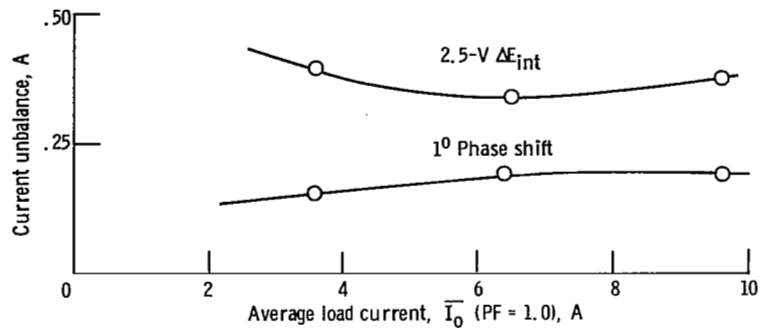


Figure 9. - Inverter current unbalance as affected by initial voltage unbalance or phase shift.

not designed for transient performance. Internal current limits (ref. 2) controlled the maximum currents, and the bus voltage was not significantly different from the non-parallel case. Switching in and out of parallel operation resulted in a 2-percent or less transient change in the output voltage. Operation during overloads and short circuits was controlled by the internal inverter current limits and was not affected by the paralleling circuit.

Three inverters were operated in parallel to produce a 3.4-kilovolt-ampere single-phase system, and six inverters were operated as a 3 phase 6.8-kilovolt-ampere Y-connected system.

## SUMMARY OF RESULTS

Load-sharing circuits developed in conjunction with a modular ac or dc pulse-width-modulated solid-state inverter-converter system were tested. The circuits were designed to provide load sharing within 10 percent of rated-load current by using feedback techniques.

In tests run on two paralleled converters, the unbalance current was 3.8 percent of the rated-load current if the converters were initially balanced and 7.4 percent for an initial output voltage unbalance of 5 volts (rated output, 150 V dc). The unbalance current of 3.8 percent for initially balanced converters was largely due to slight differences in the paralleling circuit current transducers. Also, a drift problem in the paralleling circuit caused daily output voltage variations of 5 volts, even in nonparalleled operation.

For two initially balanced inverters, the unbalance was 1.2 percent. A 5-volt (120-V rated output) initial unbalance and 1° phase shift caused a 5.6-percent current unbalance. This circuit was completely passive, required no power supply, and consumed less than 1/4 watt from the inverter output.

The analytical solution developed compared well with the test results. For example, a 4.2-percent unbalance in output current was predicted, and a 3.5-percent unbalance was measured.

The inverter paralleling required only 4 interconnections, plus ground, between inverters. The converter circuit requires only two interconnections. Phase shift in the inverter was controlled by internally synchronizing the inverters.

Transient performance of the inverters and converters was not noticeably affected by the load-sharing circuits.

Lewis Research Center,  
National Aeronautics and Space Administration,  
Cleveland, Ohio, January 19, 1972,  
112-27.

## REFERENCES

1. Gourash, Francis; Pittman, P. F.; and Heins, J. F.: Modularization of High-Power Inverters and Converters. Proceedings of the Fourth Intersociety Energy Conversion Engineering Conference. AIChE, 1969, pp. 830-838.
2. Gourash, Francis; Birchenough, Arthur G.; Pittman, Paul F.; Ravas, Richard J.; and Hall, William G.: Development and Performance of Pulse-Width-Modulated Static Inverter and Converter Modules. NASA TN D-6511, 1971.
3. Ernsberger, G. W.; Howell, H. R.; and Klingenberg, J. L.: Inverter-Converter Parallel Operation. NASA CR-1224, 1969.
4. Doughman, C. L.; Marino, B. A.; and Lenhart, N. D.: Inverter-Converter Automatic Paralleling and Protection. NASA CR-1225, 1969.